# PRODUCT SPECIFICATION

## TFT-LCD MODULE

## Model No：FRD700T40028-A

| For Customer's Acceptance | |
|---|---|
| **Approved by** | **Comment** |
| | |

| | Signature | Date |
|---|---|---|
| **Prepared by** | 陈友平 | 2021-11-15 |
| **Checked by** | 罗永 | 2021-11-15 |
| **Approved by** | 汪进 | 2021-11-15 |


深圳市福瑞达显示技术有限公司
地址：深圳市光明新区公明田寮第二工业区田荣路 68 号
Add:The 68th,Tianrong Road,Tianliao Community,Gongming Town,Guangming new district,shenzhen.
电话(Tel):0755-23422110
网址(Web):www.fridalcd.com
sales fridalcd.com

# REVISION HISTORY

| Revision | Date | Page | Revision Items | Remark |
|---|---|---|---|---|
| 1.0 | 2021/11/15 | - | First Release | |
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# 目录

## 1.Summary

This is a 6.97 inch LTPS-TFT-LCD (Thin Film Transistor Liquid Crystal Display) module with normal-black technology. It is composed of a TFT-LCD panel, LCD Driver IC with T-con integrated, POL,FPC, cover glass and a LED backlight unit.

## 2.General Specification

| Items | Specification | Remark |
|---|---|---|
| Diagonal Size | 6.97 inch | -- |
| Resolution | 1080 x RGB x 1920 | -- |
| Active Area(mm) | 86.832X154.368 | -- |
| Pixel Pitch (mm) | 80.4x80.4 | -- |
| Pixel Configuration | R.G.B. Vertical Stripe | -- |
| Technology Type | LTPS | -- |
| Display Mode | Normally Black | -- |
| Landscape or Portrait | Portrait | -- |
| Surface Treatment (Top Polarizer) | Hard Coating | -- |
| Interface | Mipi | -- |
| Color Depth | 16.7M | -- |
| Dimension (H x V x D) (mm) | 171.94x99.556x2.363 | Note1 |
| Weight (g) | TBD | Note2 |

Table 2.1 General TFT Specifications

Note1: The dimensions do not include the length of FPC, screw and component height etc.. For detail dimension, please refer to the module outline drawing.
Note2: The weight does not include the weight of protective film.

## 3.Input / Output Terminals

Mating connector type: Molex-5055514020

| Pin No. | Symbol | I/O | Description |
|---|---|---|---|
| 1 | ID(GND) | I | Check Display Source / Default--System ground |
| 2 | NC | N | Not connect, reserved for tianma test |
| 3 | NC | N | Not connect, reserved for tianma test |
| 4 | NC | N | Not connect, reserved for tianma test |
| 5 | NC | N | Not connect, reserved for tianma test |
| 6 | GND | P | Ground |
| 7 | TP_RESET | I | reset pin for touch |
| 8 | TP_I2C_SDA | I/O | I2C interface data pin for touch |
| 9 | TP_I2C_SCL | I | I2C interface clock pin for touch |
| 10 | TP_INT | O | Touch screen interrupt line |
| 11 | NC | N | Not connect |
| 12 | LED_K3 | P | LED- |
| 13 | LED_K2 | P | LED- |
| 14 | LED_K1 | P | LED- |
| 15 | LED_A | P | LED+ |
| 16 | NC | N | Not connect |
| 17 | NC | N | Not connect |
| 18 | VSN | P | Power Supply, 5.5V |
| 19 | VSP | P | Power Supply, 5.5V |
| 20 | NC | N | Not connect |
| 21 | IOVCC | P | Power Supply, 1.8V |
| 22 | RESET | I | Reset pin for display |
| 23 | TE | O | Tearing Effect output signal |
| 24 | LEDPWM | O | LCD backlight control. |
| 25 | GND | P | System ground |
| 26 | D2P | I | Positive MIPI_DSI Data differential signal input pin (Data Lane 2) |
| 27 | D2N | I | Negative MIPI_DSI Data differential signal input pin (Data Lane 2) |
| 28 | GND | P | System ground |
| 29 | D1P | I | Positive MIPI_DSI Data differential signal input pin (Data Lane 1) |
| 30 | D1N | I | Negative MIPI_DSI Data differential signal input pin (Data Lane 1) |
| 31 | GND | P | System ground |
| 32 | CLKP | I | Positive MIPI_DSI clock differential signal input pin |
| 33 | CLKN | I | Negative MIPI_DSI clock differential signal input pin |
| 34 | GND | P | System ground |
| 35 | D0P | I/O | Positive MIPI_DSI Data differential signal input pin (Data Lane 0) |
| 36 | D0N | I/O | Negative MIPI_DSI Data differential signal input pin (Data Lane 0) |
| 37 | GND | P | System ground |
| 38 | D3P | I/O | Positive MIPI_DSI Data differential signal input pin (Data Lane 3) |
| 39 | D3N | I/O | Negative MIPI_DSI Data differential signal input pin (Data Lane 3) |
| 40 | GND | P | System ground |

I/O definition: I---Input, O---Output, P---Power/Ground, N---No connection

Table 3.1.1 Pin Assignment for LCD Interface

## 4.Absolute Maximum Ratings

The following are maximum values which, if exceeded, may cause faulty operation or damage to the unit

| Parameter | Symbol | Values | | Units | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| LCD Analog Voltage | VSP | 4.5 | 6.3 | V | |
| | VSN | -6.3 | -4.5 | V | |
| LCD I/O Voltage | IOVCC | 1.65 | 1.95 | V | |
| LED Current | $I_{LED}$ | - | 16.5 | mA | |

# 5. Electrical Characteristics

## 5.1 Electrical Characteristics

| Parameter | | Symbol | Values | | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | | Min | Type | Max | | |
| LCD Input Analog Voltage | | VSP-Vss | 5.4 | 5.5 | 5.6 | V | |
| | | VSN-Vss | -5.6 | -5.5 | -5.4 | V | |
| LCD Logic I/O Voltage | | IOVCC-Vss | 1.7 | 1.8 | 1.9 | V | |
| LED Input Current | | $I_{LED}$ | - | | 16.5 | mA | |
| "H" Level Input Voltage | | $V_{IH}$ | *0.7xIOVCC* | - | *IOVCC* | V | |
| "L" Level Input Voltage | | $V_{IL}$ | *VSS* | - | *0.3xIOVCC* | V | |
| "H" Level Output Voltage | | $V_{OH}$ | *0.8xIOVCC* | - | *IOVCC* | V | |
| "L" Level Output Voltage | | $V_{OL}$ | *0.0* | - | *0.2xIOVCC* | V | |
| LCD Power Consumption | Normal | $P_N$ | - | TBD | | W | Notes 1 |
| | Sleep in | $P_D$ | - | TBD | | uW | |
| | BLU | $P_B$ | - | *971* | *1005* | mW | Notes 2 |

Notes:

(1) The specified current and power consumption are under the conditions at VSP = 5.5V,VSN=-5.5V,IOVCC = 1.8V, T = 25°C, and fv = 60 Hz, at white pattern at no touch mode

The specified current and power consumption are under the conditions at VSP = 5.5V,VSN=-5.5V,IOVCC = 1.8V, T = 25°C, and fv = 60 Hz, at R/G/B pattern (MAX)

(2) LED Backlight assumptions:19.6V（Type), 49.5mA. (7S3P LED Total Input )

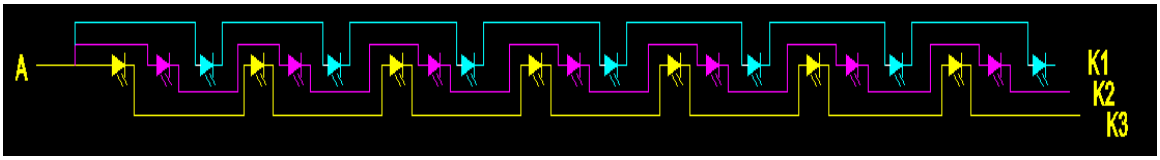
(3)Vss=GND

## 5-2. Logic Power Consumption

| Parameter | Symbol | Values | | Units | Notes |
|---|---|---|---|---|---|
| | | Typ | Max | | |
| Normal Mode | $I_{IOVCC}$ | TBD | | mA | White Pattern (no touch) |
| | $I_{Vsp}$ | TBD | | mA | |
| | $I_{Vsn}$ | TBD | | mA | |
| Sleep Mode | $I_{IOVCC}$ | TBD | | uA | |
| | $I_{Vsp}$ | TBD | | uA | |
| | $I_{Vsn}$ | TBD | | uA | |

## 5.3 DC Characteristics for Backlight Driving

| Parameter | Symbol | Values | | | Units | Notes |
|---|---|---|---|---|---|---|
| | | Min | Typ. | Max | | |
| LED Current | $I_{LED}$ | - | 16.5 | - | mA | 7S3P |
| LED Forward Voltage | $V_{LED}$ | 18.9 | 19.6 | 20.3 | V | 7S3P |




The edge-lighting type of back light unit consists of 21LEDs which is connected in serial.

## 5.4 SIGNAL TIMING SPECIFICATIONS

| ITEM | | | SYNBOL | Timing | | UUNITIT |
|---|---|---|---|---|---|---|
| **LCD** | Frame Rate | | - | TBD | TBD | Hz |
| **Timing** | DCLK | Frequency | fCLK | TBD | TBD | MHz |
| | | Period | Tclk | TBD | TBD | ns |
| | Horizontal | Horizontal total time | tHP | TBD | TBD | $t_{CLK}$ |
| | | Horizontal Active time | tHadr | TBD | TBD | $t_{CLK}$ |
| | | Horizontal Pulse Width | tHsync | TBD | TBD | $t_{CLK}$ |
| | | Horizontal Back Porch | tHBP | TBD | TBD | $t_{CLK}$ |
| | | Horizontal Front Porch | tHFP | TBD | TBD | $t_{CLK}$ |
| | Vertical | Vertical total time | tvp | TBD | TBD | $t_H$ |
| | | Vertical Active time | tVadr | TBD | TBD | $t_H$ |
| | | Vertical Pulse Width | tVsync | TBD | TBD | $t_H$ |
| | | Vertical Back Porch | tVBP | TBD | TBD | $t_H$ |
| | | Vertical Front Porch | tVFP | TBD | TBD | $t_H$ |
| **B Bit Rateit Rate** | | | TBD | TBD | TBD | TBD |
| **Pixel Format** | | | | TBD | TBD | Data bit/pixel |
| **Lane** | | | | TBD | TBD | Lane |

## 5.5 MIPI Data&CLK Line Impedance

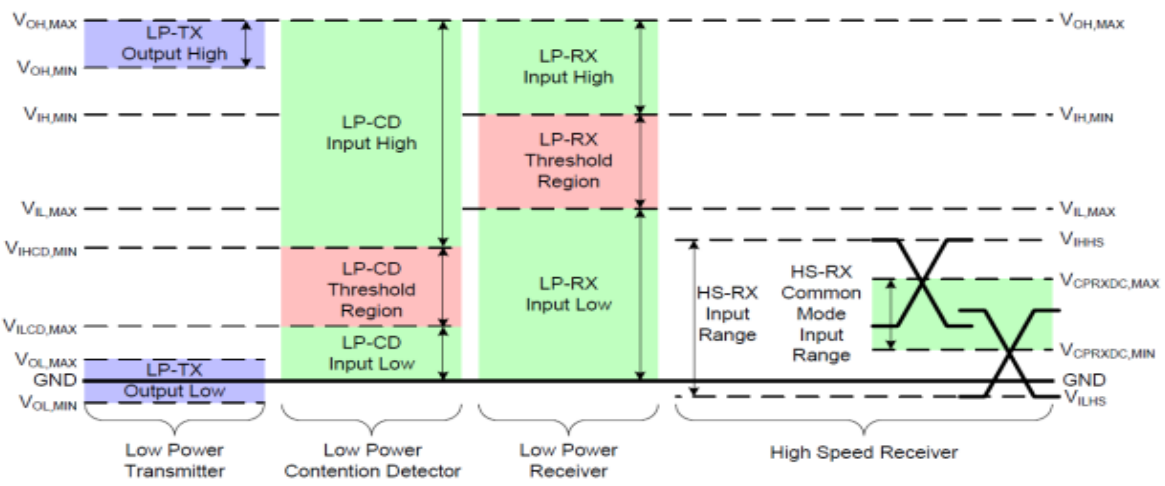
(1) MIPI Interface Timing Sequence

(a) MIPI interface DC characteristic：

| Parameter | Symbol | Condition | Specification | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Input Common Mode Voltage for Clock | $V_{CMCLK}$ | DSI-CLK+/- Note 2, Note 3 | 70 | - | 330 | mV |
| Input Common Mode Voltage for Data | $V_{CMDATA}$ | DSI-Dn+/- Note 2, Note 3, Note 5 | 70 | - | 330 | mV |
| Common Mode Ripple for Clock Equal or Less than 450MHz | $V_{CMRCLKL450}$ | DSI-CLK+/- Note 4 | -50 | - | 50 | mV |
| Common Mode Ripple for Data Equal or Less than 450MHz | $V_{CMRDATAL450}$ | DSI-Dn+/- Note 4, Note 5 | -50 | - | 50 | mV |
| Common Mode Ripple for Clock More than 450MHz (peak sine wave) | $V_{CMRCLKM450}$ | DSI-CLK+/- | - | - | 100 | mV |
| Common Mode Ripple for Data More than 450MHz (peak sine wave) | $V_{CMRDATAM450}$ | DSI-Dn+/- Note 5 | - | - | 100 | mV |
| Differential Input Low Level Threshold Voltage for Clock | $V_{THLCLK-}$ | DSI-CLK+/- | -70 | - | - | mV |
| Differential Input Low Level Threshold Voltage for Data | $V_{THLDATA-}$ | DSI-Dn+/- Note 5 | -70 | - | - | mV |
| Differential Input High Level Threshold Voltage for Clock | $V_{THHCLK+}$ | DSI-CLK+/- | - | - | 70 | mV |
| Differential Input High Level Threshold Voltage for Data | $V_{THHDATA+}$ | DSI-Dn+/- Note 5 | - | - | 70 | mV |
| Single-ended Input Low Voltage | $V_{ILHS}$ | DSI-CLK+/-, DSI-Dn+/- Note 3, Note 5 | -40 | - | - | mV |
| Single-ended Input High Voltage | $V_{IHHS}$ | DSI-CLK+/-, DSI-Dn+/- Note 3, Note 5 | - | - | 460 | mV |
| Differential Termination Resistor | $R_{TERM}$ | DSI-CLK+/-, DSI-Dn+/- Note 5 | 80 | 100 | 125 | Ω |
| Single-ended Threshold Voltage for Termination Enable | $V_{TERM-EN}$ | DSI-CLK+/-, DSI-Dn+/- Note 5 | - | - | 450 | mV |
| Termination Capacitor | $C_{TERM}$ | DSI-CLK+/-, DSI-Dn+/- Note 5, Note 6 | - | - | 60 | pF |

Note:

1. Ta = -30 to 70°C, VDDI=1.65V ~ 1.95V, AVDD=4.5V ~ 6.3V, AVEE=-4.5V ~ -6.3V, VSS=AVSS=0V.
2. Includes 50mV (-50mV to 50mV) ground difference.
3. Without VCMRCLKM450/VCMRDATAM450.
4. Without 50mV (-50mV to 50mV) ground difference.
5. n = 0,1,2,3
6. For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.



(b) MIPI Timing Characteristics

**High Speed Mode – Clock Channel Timing**

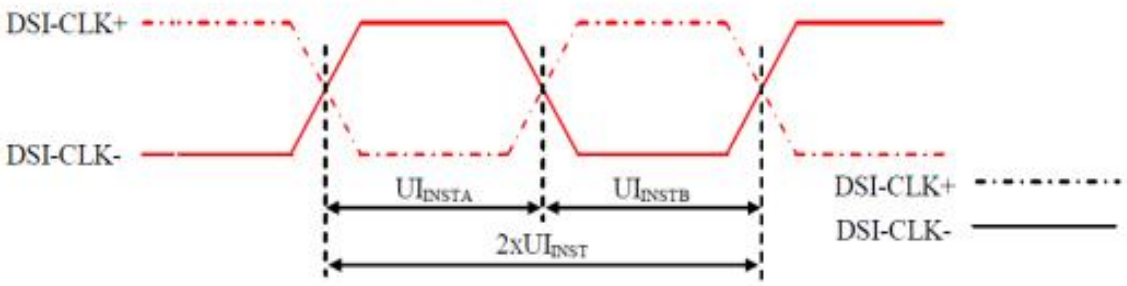



**Figure 106. DSI Clock Channel Timing**

**Table 45. DSI Clock Channel Timing**

| Signal | Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|---|
| DSI-CLK+/- | $2xUI_{INST}$ | Double UI instantaneous | 2 | 25 | ns |
| DSI-CLK+/- | $UI_{INSTA}$, $UI_{INSTB}$ | UI instantaneous Half | 1 | 12.5 | ns |

Note: $UI_{INST} = UI_{INSTA} = UI_{INSTB}$

**High Speed Mode – Data Clock Channel Timing**

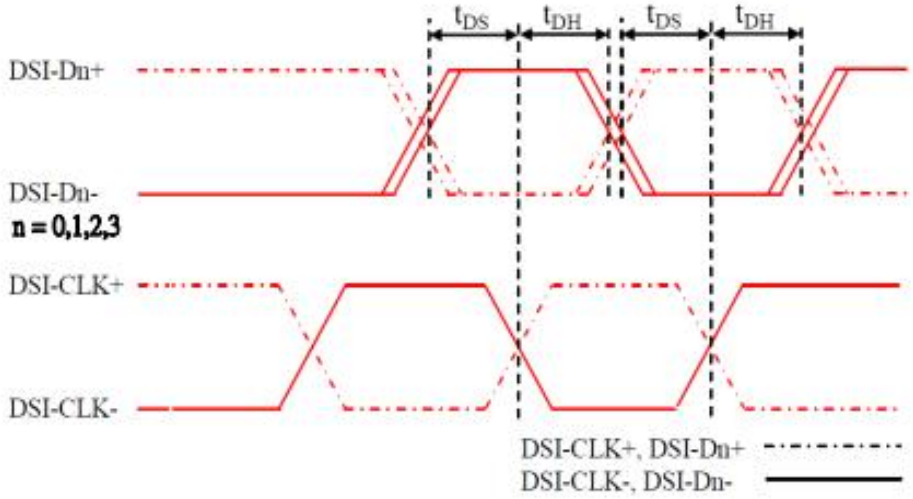



**Figure 107. DSI Data to Clock Channel Timings**

**Table 46. DSI Data to Clock Channel Timings**

| Signal | Symbol | Parameter | Min. | Max. |
|---|---|---|---|---|
| DSI-Dn+/- (n=0,1,2,3) | $t_{DS}$ | Data to Clock Setup time | 0.15xUI | - |
| | $t_{DH}$ | Clock to Data Hold Time | 0.15xUI | - |

## High Speed Mode – Rise and Fall Timings

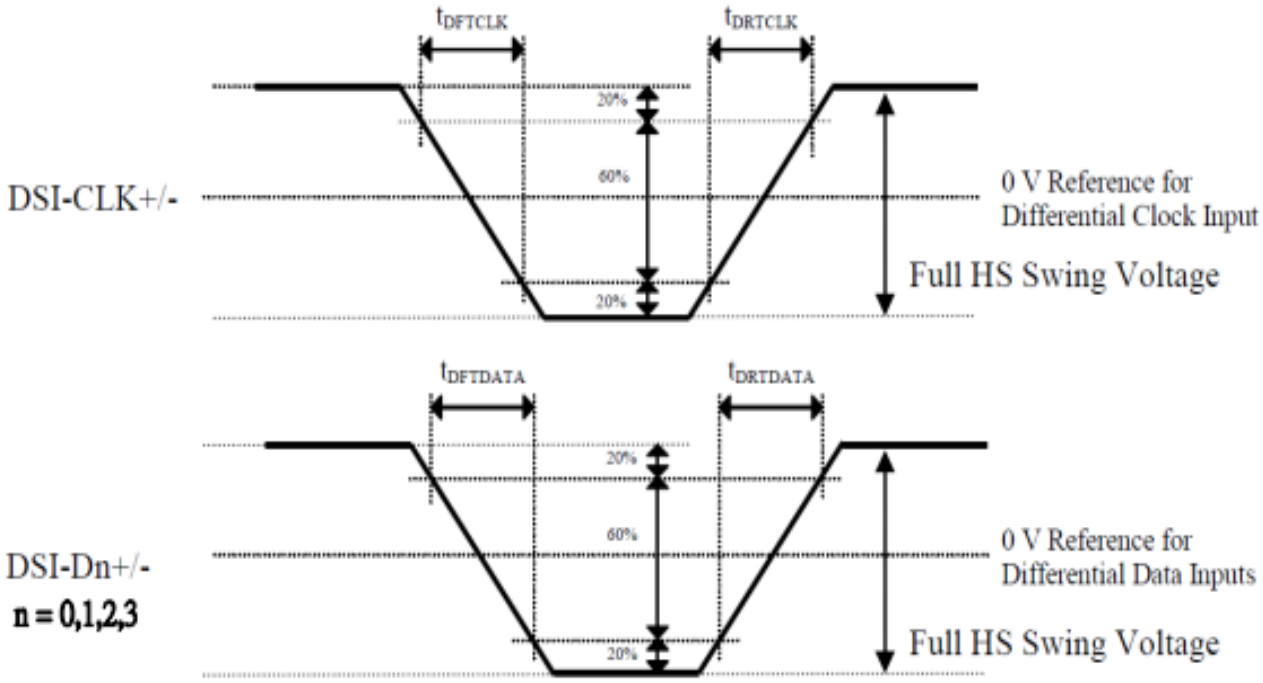



**Figure 108. Rise and Fall Timings on Clock and Data Channels**

**Table 47. Rise and Fall Timings on Clock and Data Channels**

| Parameter | Symbol | Condition | Specification | | |
|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. |
| Differential Rise Time for Clock | $t_{DRTCLK}$ | DSI-CLK+/- | 150 ps | - | 0.3UI |
| Differential Rise Time for Data | $t_{DRTDATA}$ | DSI-Dn+/- (n=0,1,2,3) | 150 ps | - | 0.3UI |
| Differential Fall Time for Clock | $t_{DFTCLK}$ | DSI-CLK+/- | 150 ps | - | 0.3UI |
| Differential Fall Time for Data | $t_{DFTDATA}$ | DSI-Dn+/- (n=0,1,2,3) | 150 ps | - | 0.3UI |

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the MCU to the Display Module sequence below.

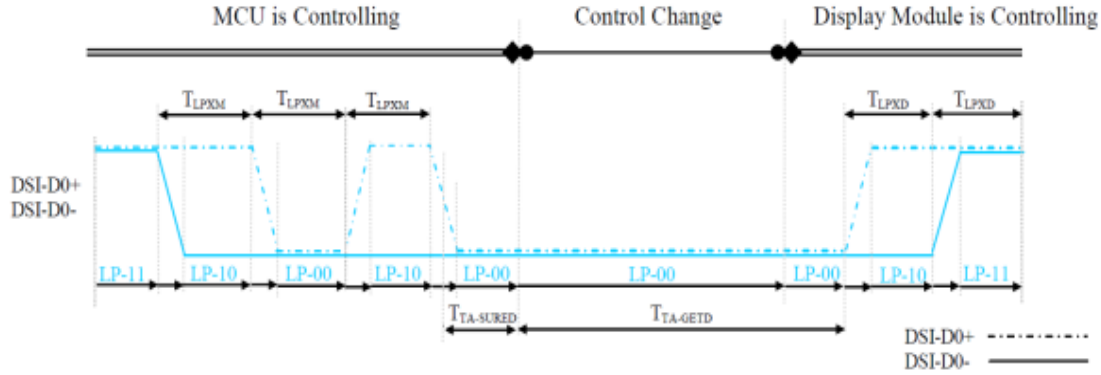



**Figure 109. BTA from the MCU to the Display Module**

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the Display Module to the MCU sequence below.

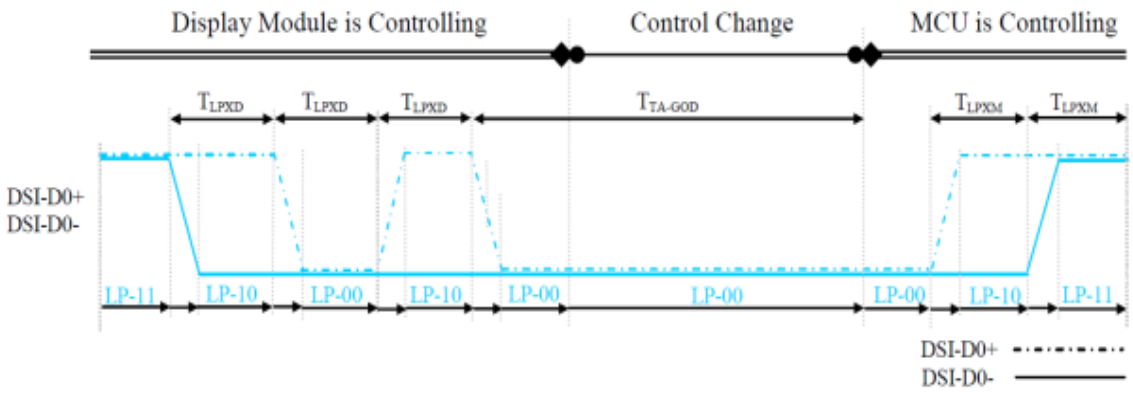



**Figure 110. BTA from the Display Module to the MCU**

**Table 48. Low Power State Period Timings – A**

| Signal | Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|---|
| DSI-D0+/- | $T_{LPXM}$ | Length of LP-00, LP-01, LP-10 or LP-11 periods<br>MCU → Display Module | 50 | 75 | ns |
| DSI-D0+/- | $T_{LPXD}$ | Length of LP-00, LP-01, LP-10 or LP-11 periods<br>Display Module → MCU | 50 | 75 | ns |
| DSI-D0+/- | $T_{TA-SURED}$ | Time-out before the Display Module starts driving | $T_{LPXD}$ | $2*T_{LPXD}$ | ns |

**Table 49. Low Power State Period Timings – B**

| Signal | Symbol | Description | Time | Unit |
|---|---|---|---|---|
| DSI-D0+/- | $T_{TA-GETD}$ | Time to drive LP-00 by Display Module | $5*T_{LPXD}$ | ns |
| DSI-D0+/- | $T_{TA-GOD}$ | Time to drive LP-00 after turnaround request – MCU | $4*T_{LPXD}$ | ns |

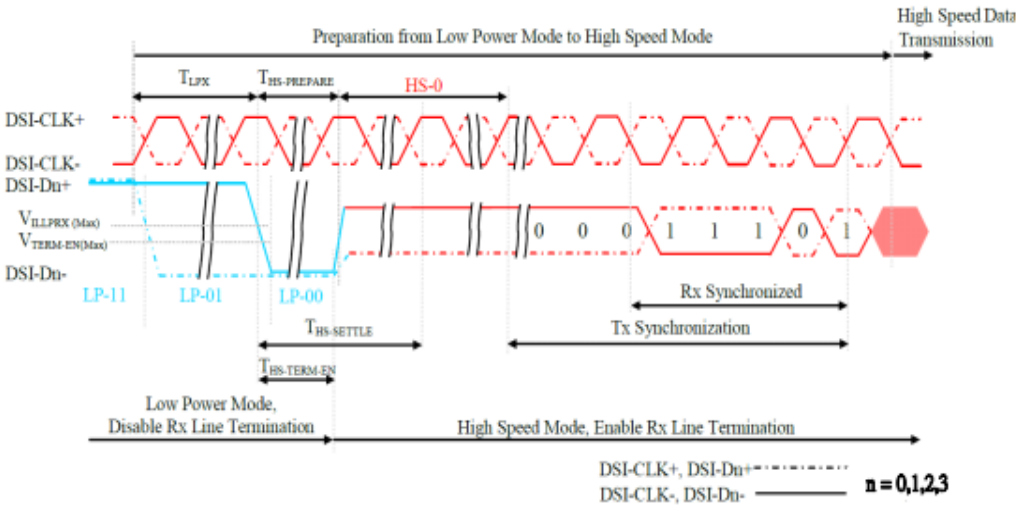



**Figure 111. Data Lanes – Low Power Mode to High Speed Mode Timings**

**Table 50. Data Lanes – Low Power Mode to High Speed Mode Timings**

| Signal | Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|---|
| DSI-Dn+/- (n=0,1,2,3) | $T_{LPX}$ | Length of any Low Power State Period | 50 | - | ns |
| DSI-Dn+/- (n=0,1,2,3) | $T_{HS-PREPARE}$ | Time to drive LP-00 to prepare for HS Transmission | 40+4xUI | 85+6xUI | ns |
| DSI-Dn+/- (n=0,1,2,3) | $T_{HS-TERM-EN}$ | Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX | - | 35+4xUI | ns |

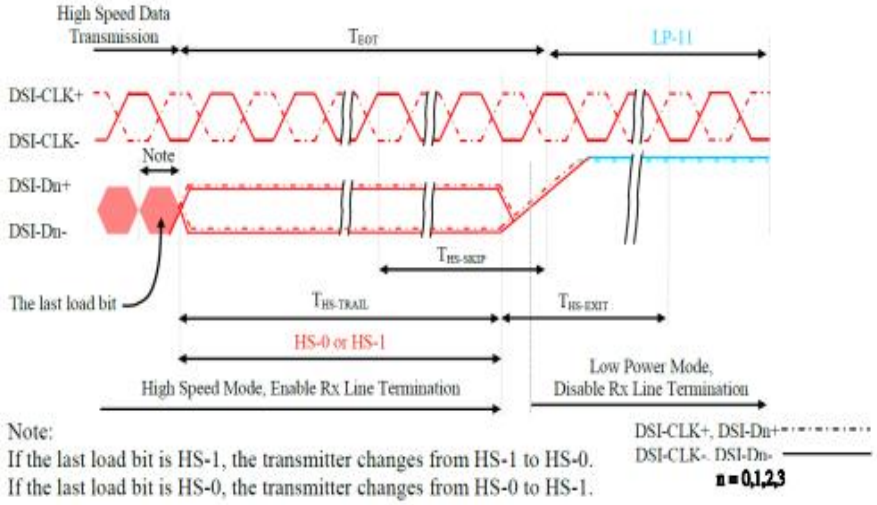



**Figure 112. Data Lanes – High Speed Mode to Low Power Mode Timings**

**Table 51. Data Lanes – High Speed Mode to Low Power Mode Timings**

| Signal | Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|---|
| DSI-Dn+/- (n=0,1,2,3) | $T_{HS-SKIP}$ | Time-Out at Display Module to ignore transition period of EoT | 40 | 55+4xUI | ns |
| DSI-Dn+/- (n=0,1,2,3) | $T_{HS-EXIT}$ | Time to driver LP-11 after HS burst | 100 | - | ns |
| DSI-Dn+/- (n=0,1,2,3) | $T_{HS-TRAIL}$ | Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst | max(8*UI, 60ns+4*UI) | - | ns |

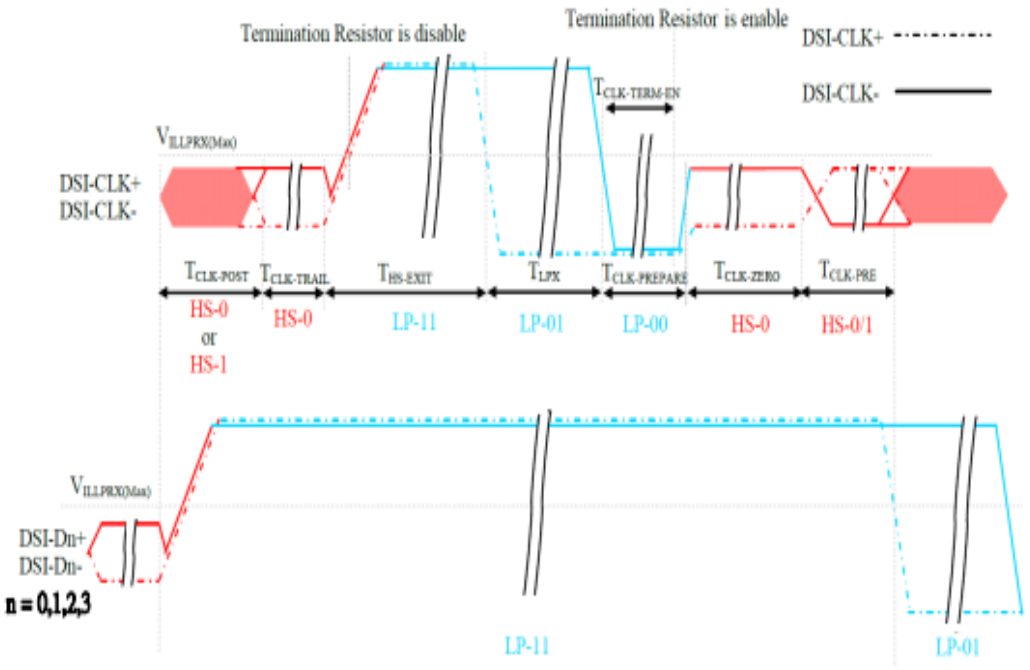



**Figure 113. Clock Lanes – High Speed Mode to/from Low Power Mode Timings**

**Table 52. Clock Lanes – High Speed Mode to/from Low Power Mode Timings**

| Signal | Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|---|
| DSI-CLK+/- | $T_{CLK-POST}$ | Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode | 60+52xUI | - | ns |
| DSI-CLK+/- | $T_{CLK-TRAIL}$ | Time to drive HS differential state after last payload clock bit of a HS transmission burst | 60 | - | ns |
| DSI-CLK+/- | $T_{HS-EXIT}$ | Time to drive LP-11 after HS burst | 100 | - | ns |
| DSI-CLK+/- | $T_{CLK-PREPARE}$ | Time to drive LP-00 to prepare for HS transmission | 38 | 95 | ns |
| DSI-CLK+/- | $T_{CLK-TERM-EN}$ | Time-out at Clock Lane to enable HS termination | - | 38 | ns |
| DSI-CLK+/- | $T_{CLK-PREPARE}$ | Minimum lead HS-0 drive period before starting Clock | 300 | - | ns |
| DSI-CLK+/- | $T_{CLK-PRE}$ | Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode | 8xUI | - | ns |

(2)Reset Input Timing

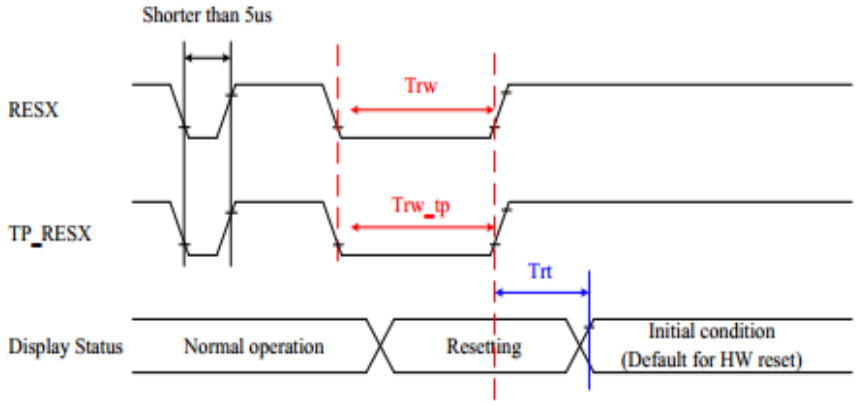



**Figure 97. Reset Timing**

**Table 41. Reset Timing**

| Signal | Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|---|
| RESX | Trw | Reset pulse duration | 10 | - | us |
| | Trt | Reset cancel | 35 (Note 1,5) | - | ms |
| | | | 150 (Note 1,6,7) | - | ms |
| TP_RESX | Trw_tp | Reset pulse duration | 10 | - | us |

Note:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM to registers. This loading is done every time when there is H/W reset cancel time (Trt) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the following table.

**Table 42. Reset Description**

| RESX | Action |
|---|---|
| Shorter than 5us | Reset Rejected |
| Longer than 9us | Reset |
| Between 5us and 9us | Reset starts |

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode.) and return to default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown in following figure.

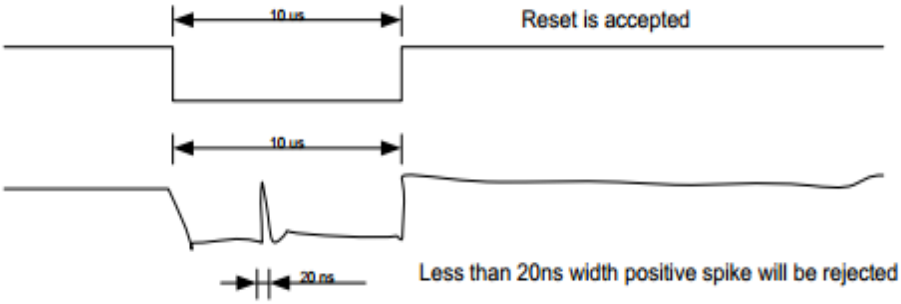



**Figure 98. Positive Noise Pulse during Reset Low**

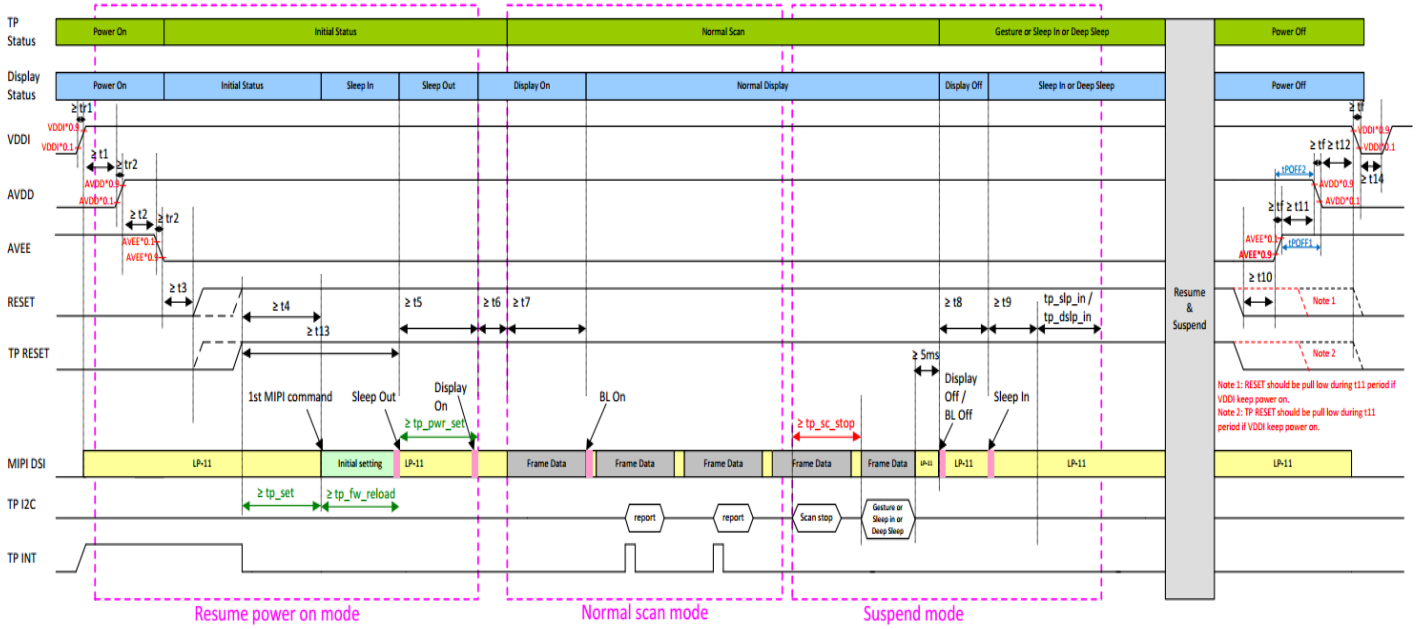
5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending other commands. Also Sleep Out command (11h) cannot be sent for 120msec.

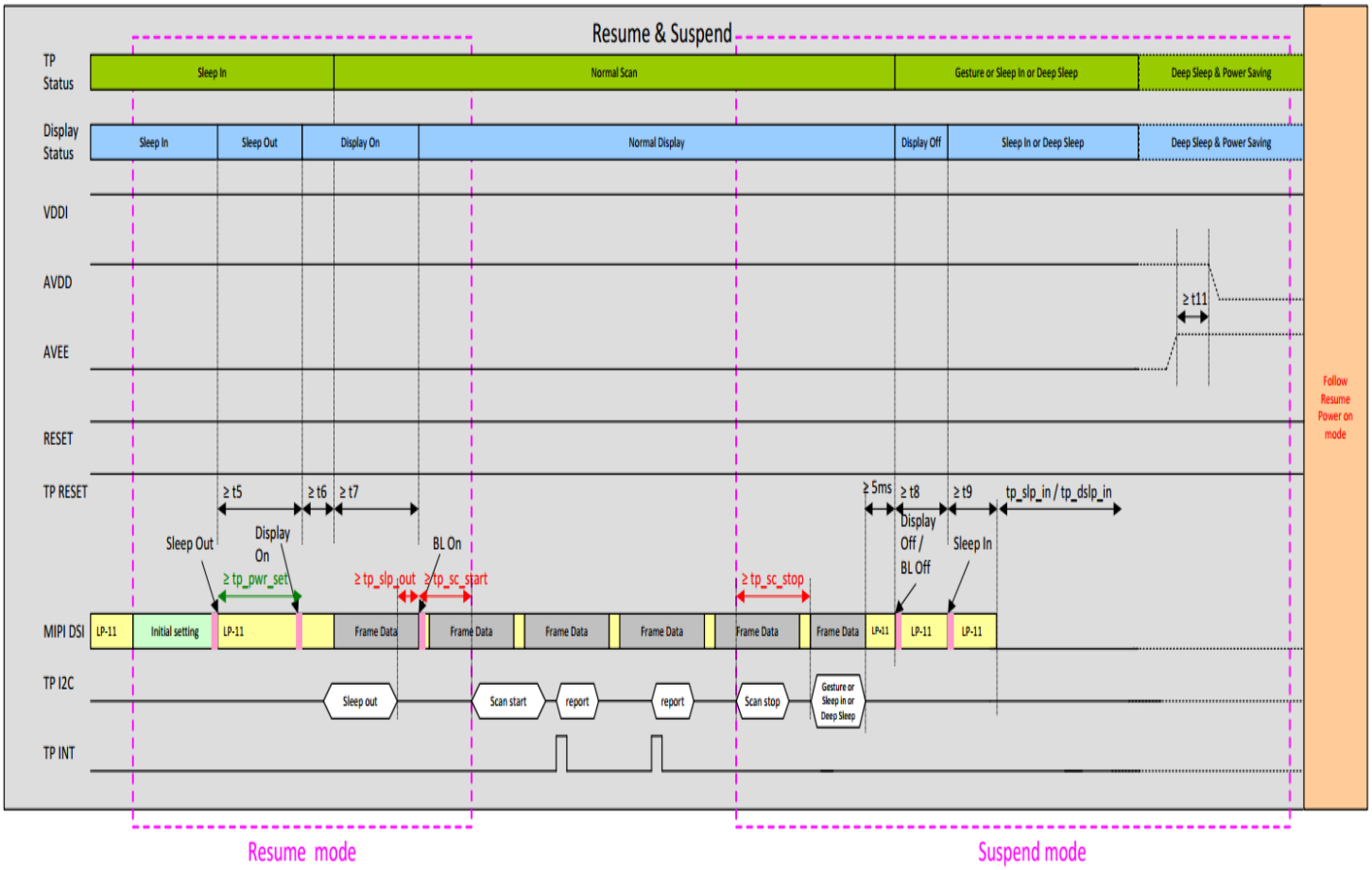
## 5.6 Recommended Power Sequence

### 5.6.1 Power sequence

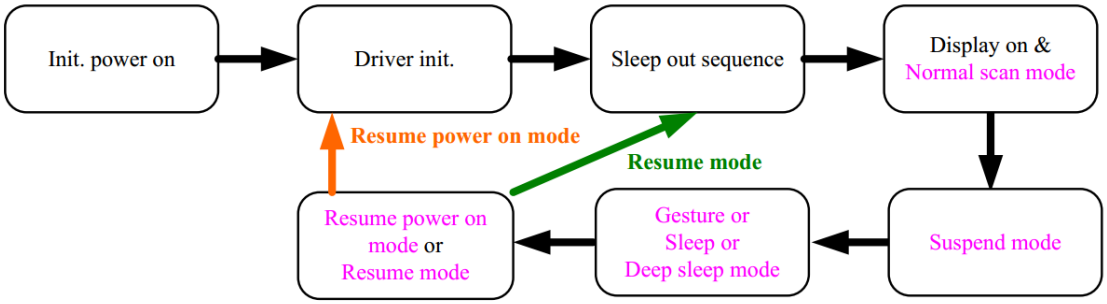
1.1 Normal mode

The power sequence of normal mode






The flow chart of normal mode



| Normal Mode | Min. | Typ. | Max. | Note |
|---|---|---|---|---|
| tr1 (ms) | 0.05 | - | 20 | VDDI rising time |
| tr2 (ms) | 0.05 | - | 20 | AVDD, AVEE rising time |
| tf (ms) | 0.05 | - | 20 | External power falling time |
| t1 (ms) | 1 | - | - | |
| t2 (ms) | 1 | - | - | |
| t3 (ms) | 1 | - | - | |
| t4 (ms) | 10 | - | - | DDI OTP reload.<br>RESET to first command in display sleep in mode time. |
| t5 (ms) | 60 | - | - | Sleep Out Sequence |
| t6 (ms) | 0 | - | - | |
| t7 (ms) | 50 | - | - | |
| t8 (ms) | 16.67 | - | - | Depend on frame rate. |
| T9 (ms) | 80 | - | - | Sleep In Sequence<br>*The min. time of sleep in should be longer than panel power off request |
| t10 (ms) | 1 | - | - | |
| t11 (ms) | 0 | - | - | AVDD≧\|AVEE\| *No limitation for t11 |
| tPOFF2 (ms) | 0.05 | - | - | AVEE 90% to AVDD 90% |
| tPOFF1 (ms) | 0.05 | - | - | AVEE 10% to AVDD 10% |
| t12 (ms) | 0 | - | - | |
| t13 (ms) | 47 | - | - | TP RESET to 1st TP CMD delay time |
| t14(ms) | 10 | - | - | Delay time between VDDI power off to power on |
| tp_set (ms) | 10 | - | - | TP OTP reload |
| tp_fw_reload (ms) | 37 | - | - | Flash reload |
| tp_pwr_set (ms) | 60 | - | - | Initial setting |
| tp_slp_out (ms) | 0 | - | - | Resume timing |
| tp_sc_start (ms) | 35 | - | - | |
| tp_sc_stop (ms) | 35 | - | - | |
| tp_slp_in (ms) | 35 | - | - | Entry Sleep mode wait time |
| tp_dslp_in (ms) | 35 | - | - | Entry Deep Sleep mode wait time |

*Resume Power On mode : If resume AVDD & AVEE power off, please follow Resume power on mode.

* Before VDDI power on, please make sure VDDI, VDD, VDD_TP are under 100mV for 10ms.

* When sleep in mode, RESET & TP RESET can keep low after AVDD & AVEE power off.

* Exit Deep Sleep mode : Entry deep sleep mode and AVDD & AVEE power off, please follow Resume power on mode.

Figure 1 Interface power sequence

Note：AVDD=VSP,AVEE=VSN,VDDI=IOVCC

## 6.Optical Characteristics

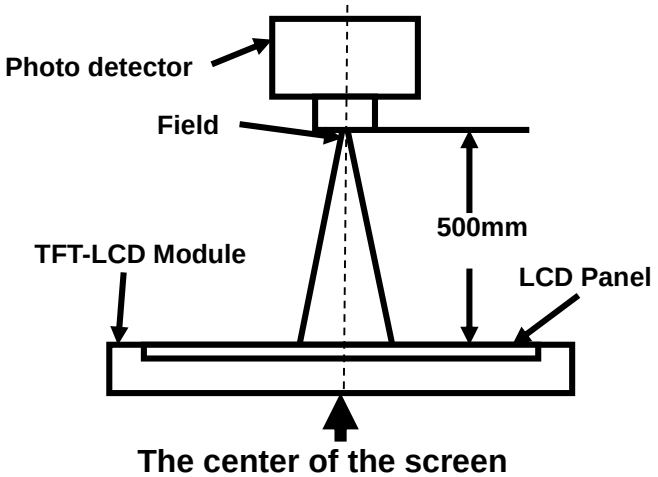
| Item | | Symbol | Condition | Min | Typ | Max | Unit | Remark |
|---|---|---|---|---|---|---|---|---|
| Viewing Angle | | θU | CR >10 0/90/180/270 | 80 | -- | -- | ° | Note2 |
| | | θD | | 80 | -- | -- | | |
| | | θL | | 80 | -- | -- | | |
| | | θR | | 80 | -- | -- | | |
| Contrast Ratio | | CR | Vertical,25℃ | 800 | 1000 | -- | -- | Note 1,3 |
| Response Time | | Tr+Tf | 25℃ | -- | -- | 30 | ms | Note1、4 |
| Chromaticity | White | X | CIE1931-XYZ | 0.280 | 0.310 | 0.340 | -- | Note1、5 |
| | | Y | | 0.293 | 0.323 | 0.353 | | |
| | Red | X | | 0.601 | 0.631 | 0.661 | | |
| | | Y | | 0.298 | 0.328 | 0.358 | | |
| | Green | X | | 0.254 | 0.284 | 0.314 | | |
| | | Y | | 0.571 | 0.601 | 0.631 | | |
| | Blue | X | | 0.128 | 0.158 | 0.188 | | |
| | | Y | | 0.022 | 0.052 | 0.082 | | |
| | NTSC | | | 65 | 70 | -- | % | |
| Luminance | | L | 25℃ | 380 | 450 | -- | cd/m² | Note1、7 |
| Uniformity | | White | | 75% | 80% | -- | % | Note1、6 |

Test Conditions:

1. The ambient temperature is 25℃.

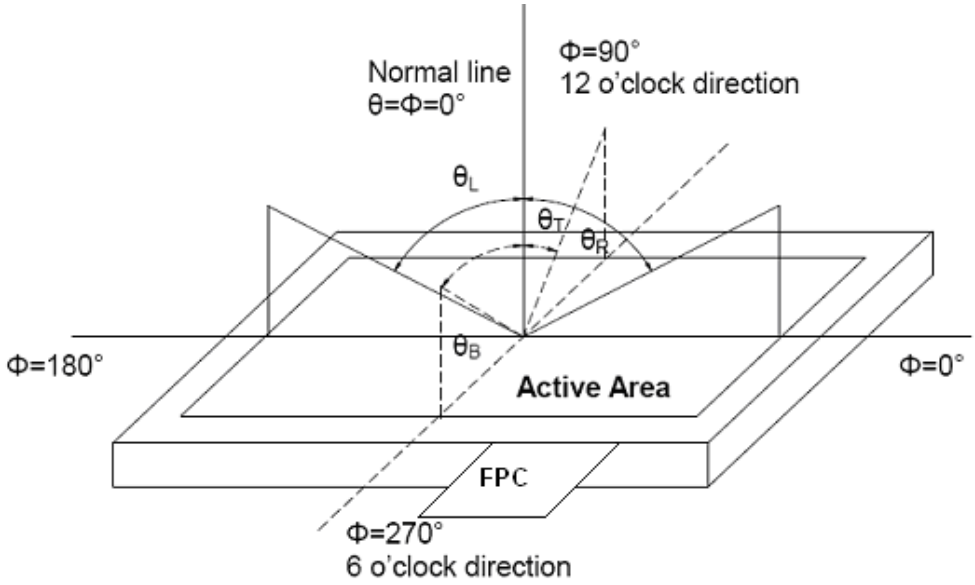
Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 Minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Note 2: Definition of viewing angle range and measurement system.

viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80)。




Note 3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

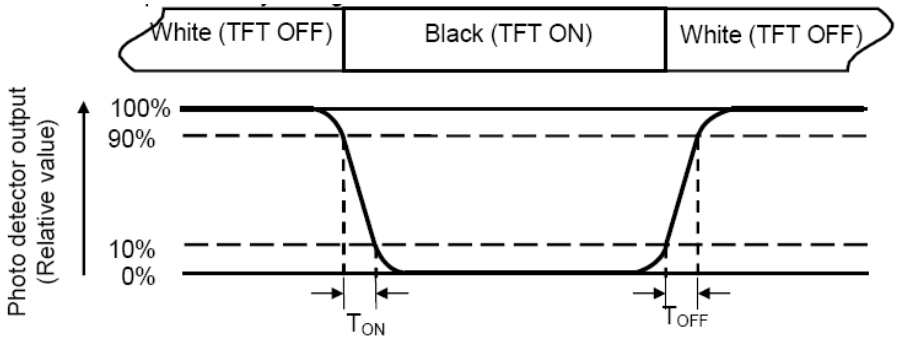
“White state “: The state is that the LCD should drive by Vwhite.

“Black state”: The state is that the LCD should drive by Vblack.

Vwhite: To be determined Vblack: To be determined.

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time ($T_{ON}$) is the time between photo detector output intensity changed from 90% to 10%. And fall time ($T_{OFF}$) is the time between photo detector output intensity changed from 10% to 90%.




Note 5: Definition of color chromaticity (CIE1931)

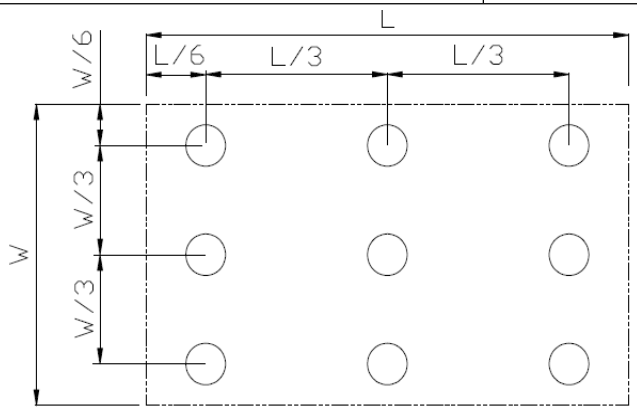
Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/ Lmax

L-------Active area length W----- Active area width




Lmax: The measured Maximum luminance of all measurement position.

Lmin: The measured Minimum luminance of all measurement position.

Note 7: Definition of Luminance:

Measure the luminance of white state at center point.

## 7.Reliability Test

**Contents of Reliability Test**

| No | Test Item | Test condition | Criterion |
|---|---|---|---|
| 1 | High Temperature Storage | Ta = +80℃, 240 hours | |
| 2 | Low Temperature Storage | Ta = -30℃, 240 hours | |
| 3 | High Temperature Operation | Ta = +70℃, 240 hours | |
| 4 | Low Temperature Operation | Ta = -20℃, 240 hours | |
| 5 | High Temperature & Humidity Operation (operational) | Ta = +60℃, 90% RH max,240 hours | |
| 6 | Thermal Shock (non-operational) | -30℃ 30 min~+80℃ 30 min, Change time:5min, 20 Cycle | |
| 7 | ESD (operational) | C=150pF,R=330Ω,5point/panel<br>Air:±8Kv,5times;<br>Contact:±4Kv,5times<br>(Environment:15℃~35℃,30%~60%.86Kpa~106Kpa) | |
| 8 | Package Drop Test | Height: 60 cm,1 corner, 3 edges, 6 surfaces | |
| 9 | Image sticking | 25℃, 6*8 chess board, Burn-in time:1h, Judge at 5min @127 gray pattern | JND≤2.3 |

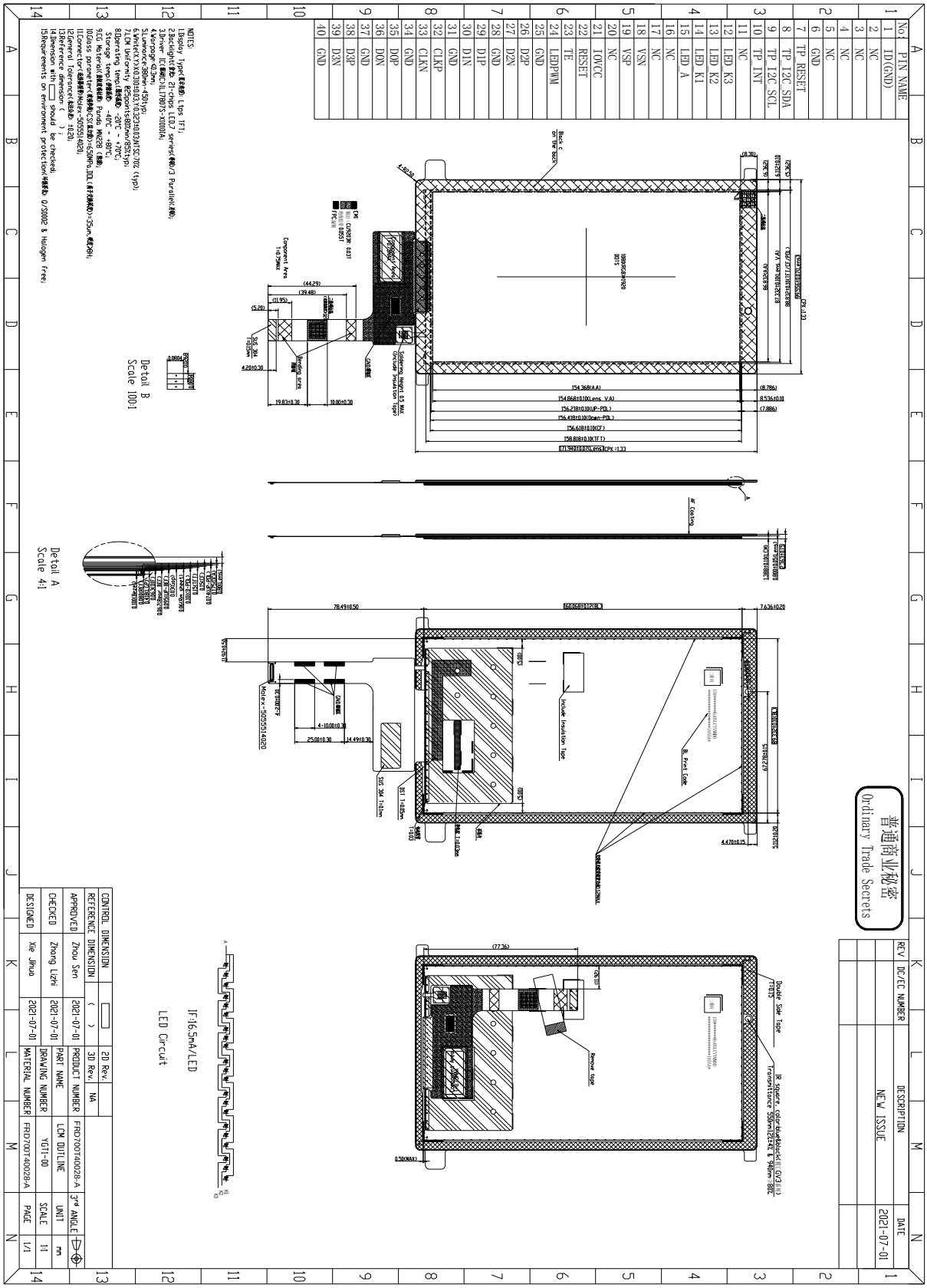
Note1: Ta is the ambient temperature of samples.

Note2: Before cosmetic and function test, the product must have enough recovery time, at least 24 hours at room

temperature.

Note3: ND5% Waving can be ignored after 48 h.

## 8.Mechanical Drawing



TBD

## 9.1 Packaging Material (Per Carton )

TBD

## 9.2.Packaging Specification and Quantity

TBD

## 9.3 stack placement

TBD

# 10.Precautions for Use of LCD Module

## 10.1 Handling Precautions

(1) The display panel is made of glass. Do not subject it to mechanical shock by dropping it, etc.
(2) If the display panel is damaged and the liquid crystal fluid inside it leaks out be sure not to get any in your mouth. If the fluid comes into contact with your skin or clothes promptly wash it off using soap and water.
(3) Do not apply excessive force to the display surface or the bezel since this may cause the color tone to vary.
(4) The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle the polarizer carefully.
(5) If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If it is still not completely clear use a moist cloth with one of the following solvents:

- Isopropyl alcohol

Solvents other than those mentioned above may damage the polarizer. Specifically, do not use the following:

- Water
- Ketone
- Aromatic solvents

(6) POL surface temperature shall not exceed 95℃ when the product is used or tested.
(7) The storage or use environment must not contain an acid or base environment. for example,NH3,SO2…
(8) Do not attempt to disassemble the LCD Module.
(9) If the logic circuitry is powered off, do not apply the input signals.
(10) To prevent destruction of the module by static electricity, be careful to maintain an optimum work environment.
(11) Be sure to ground your body when handling the LCD Modules.
(12) Tools used for assembly, such as soldering irons, must be properly grounded.
(13) To reduce the amount of static electricity generated, do not conduct assembly or other work under very low humidity conditions.
(14) The LCD Module is covered with a film to protect the display surface. Be careful when peeling off this protective film since static electricity may be generated.

## 10.2 Storage precautions

(1) When storing the LCD modules avoid exposure to direct sunlight or to the light of fluorescent lamps.
(2) The LCD modules should be stored within the rated storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:
Temperature: 15 ~ 35 degree C (or at least Temp. 10 ~ 40 degree C / Humidity 25% ~ 75%), for National Std. recommendation
(3) The LCD modules should be stored in a room without acid, alkali or other harmful gases.

## 10.3 Transportation Precautions

The LCD modules should not be dropped or subject to violent mechanical shock during transportation. Also they should avoid excessive pressure, water, high humidity and direct sunlight.

## 11.Contact Us

TBD